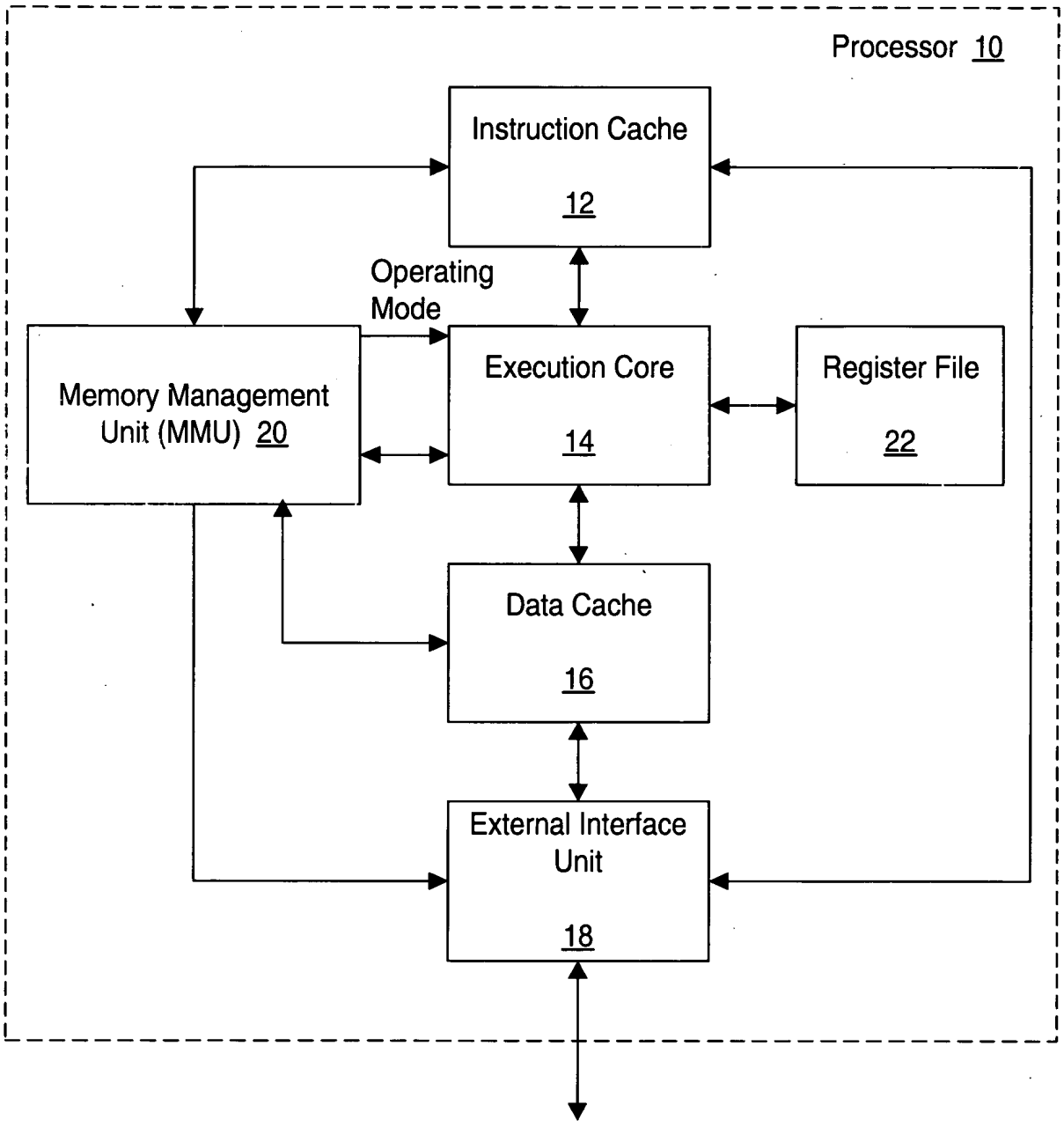
Processor 10
Instruction Cache
12
Operating
Mode
Memory Management
Unit (MMU) 20
Execution Core
14
Register File
22
Data Cache
16
External Interface
Unit
18

Fig. 1

	31	16	15	8	7	0
EAX			AH (100+!P)		AL (000)	
ECX			CH (101+!P)		CL (001)	
EDX			DH (110+!P)		DL (010)	
EBX			BH (111+!P)		BL (011)	
ESP					SPL (100+P)	
EBP					BPL (101+P)	
ESI					SIL (110+P)	
					DIL (111+P)	

Note: "+P" = Instruction Includes Register Address Prefix Byte
"+!P" = Instruction Excludes Register Address Prefix Byte

Fig. 2

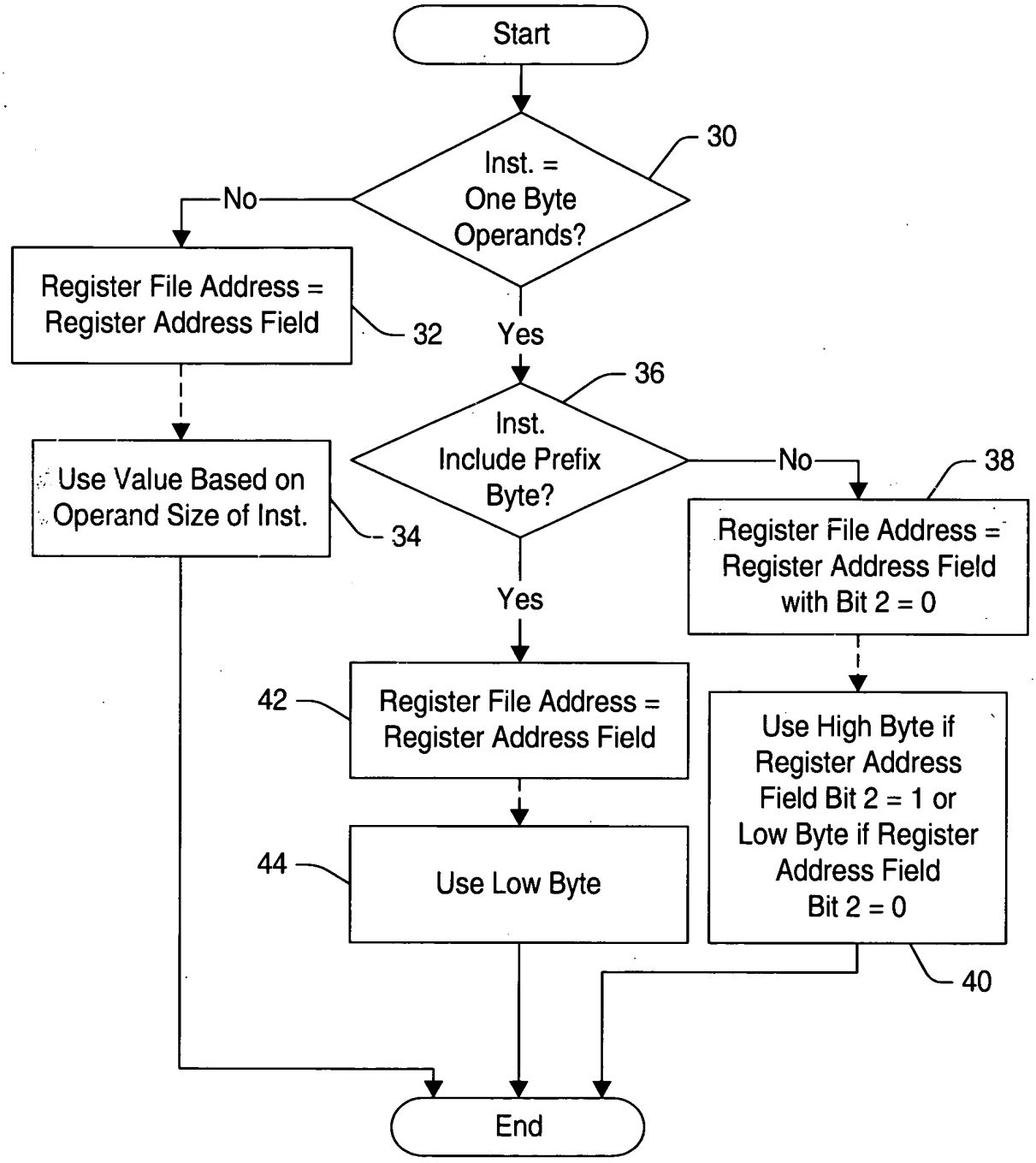
Start
Inst. = One Byte Operands?
30
No
Yes
Register File Address = Register Address Field
32
Use Value Based on Operand Size of Inst.
34
Inst. Include Prefix Byte?
36
No
Yes
38
Register File Address = Register Address Field with Bit 2 = 0
Use High Byte if Register Address Field Bit 2 = 1 or Low Byte if Register Address Field Bit 2 = 0
40
42
Register File Address = Register Address Field
44
Use Low Byte
End

Fig. 3

	31 or 63 — 16	15 — 8	7 — 0
EAX		AH (x100+!P)	AL (0000+P or x000+!P)
ECX		CH (x101+!P)	CL (0001+P or x001+!P)
EDX		DH (x110+!P)	DL (0010+P or x010+!P)
EBX		BH (x111+!P)	BL (0011+P or x011+!P)
ESP			SPL (0100+P)
EBP			BPL (0101+P)
ESI			SIL (0110+P)
EDI			DIL (0111+P)
R8			R8B (1000+P)
R9			R9B (1001+P)
R10			R10B (1010+P)
R11			R11B (1011+P)
R12			R12B (1100+P)
R13			R13B (1101+P)
R14			R14B (1110+P)
R15			R15B (1111+P)

Note: "+P" = Instruction Includes Register Address Prefix Byte
"+!P" = Instruction Excludes Register Address Prefix Byte

Fig. 4

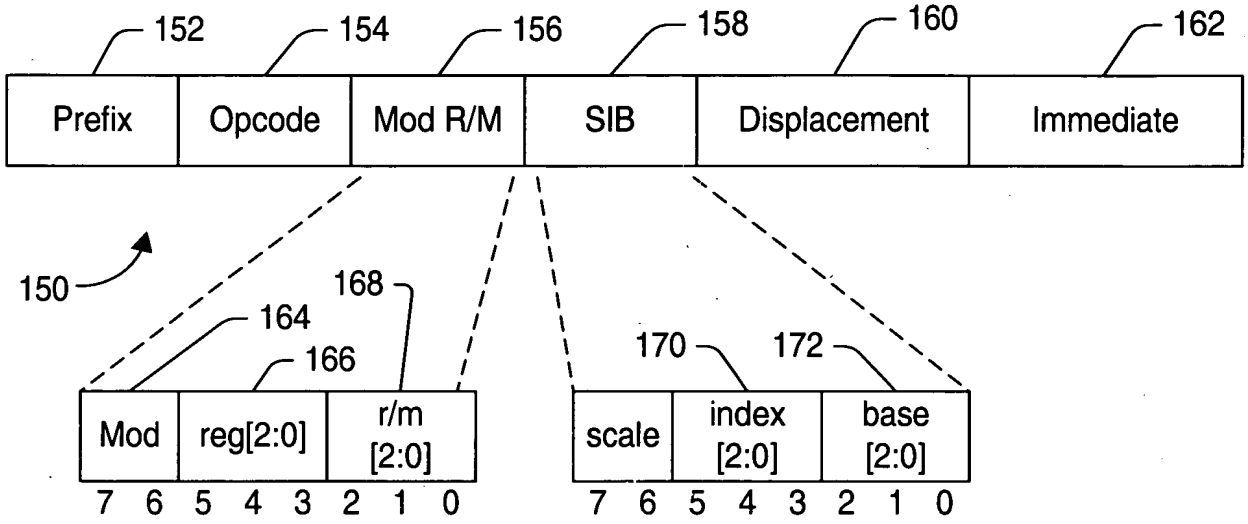
152
154
156
158
160
162
Prefix
Opcode
Mod R/M
SIB
Displacement
Immediate
150
164
168
166
170
172
Mod
reg[2:0]
r/m
[2:0]
scale
index
[2:0]
base
[2:0]
7 6 5 4 3 2 1 0
7 6 5 4 3 2 1 0

Fig. 5

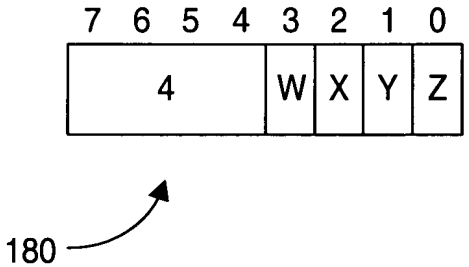
7 6 5 4 3 2 1 0
4
W
X
Y
Z
180

Fig. 6

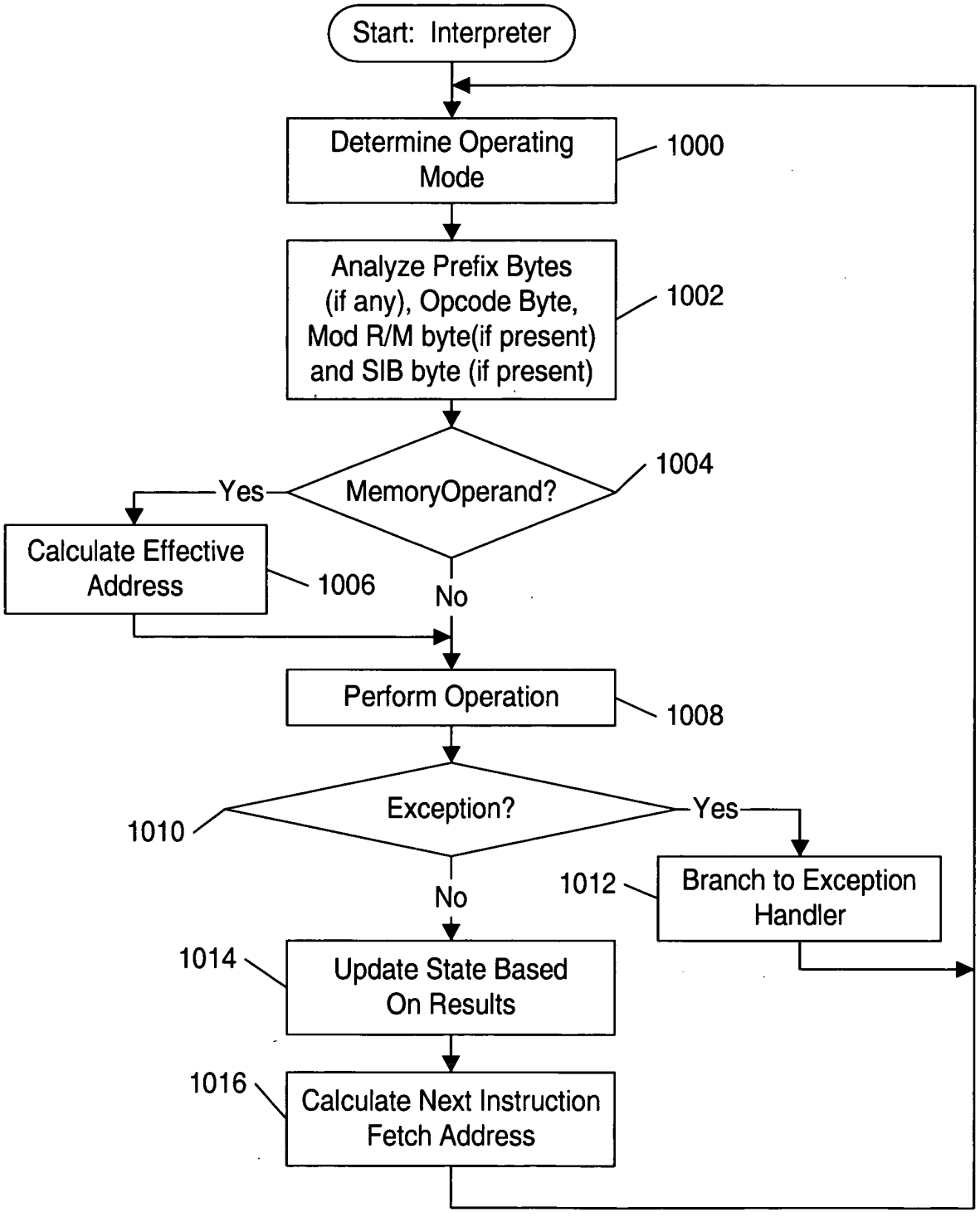
Start: Interpreter
Determine Operating Mode
1000
Analyze Prefix Bytes (if any), Opcode Byte, Mod R/M byte(if present) and SIB byte (if present)
1002
MemoryOperand?
1004
Yes
Calculate Effective Address
1006
No
Perform Operation
1008
Exception?
1010
Yes
Branch to Exception Handler
1012
No
Update State Based On Results
1014
Calculate Next Instruction Fetch Address
1016

Fig. 7

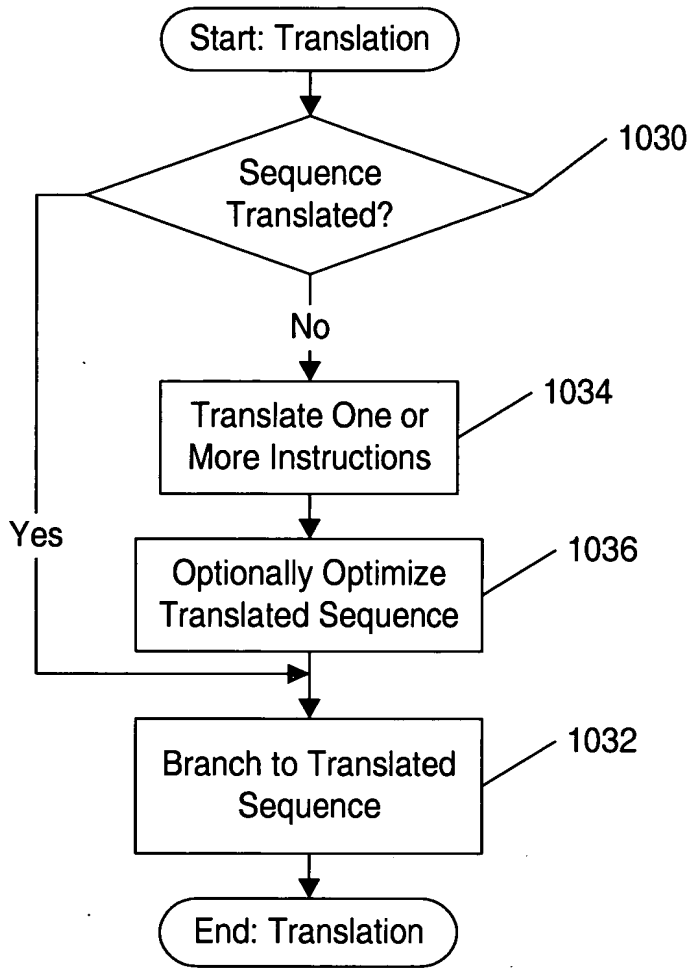
Start: Translation
Sequence Translated?
1030
No
Translate One or More Instructions
1034
Yes
Optionally Optimize Translated Sequence
1036
Branch to Translated Sequence
1032
End: Translation

Fig. 8

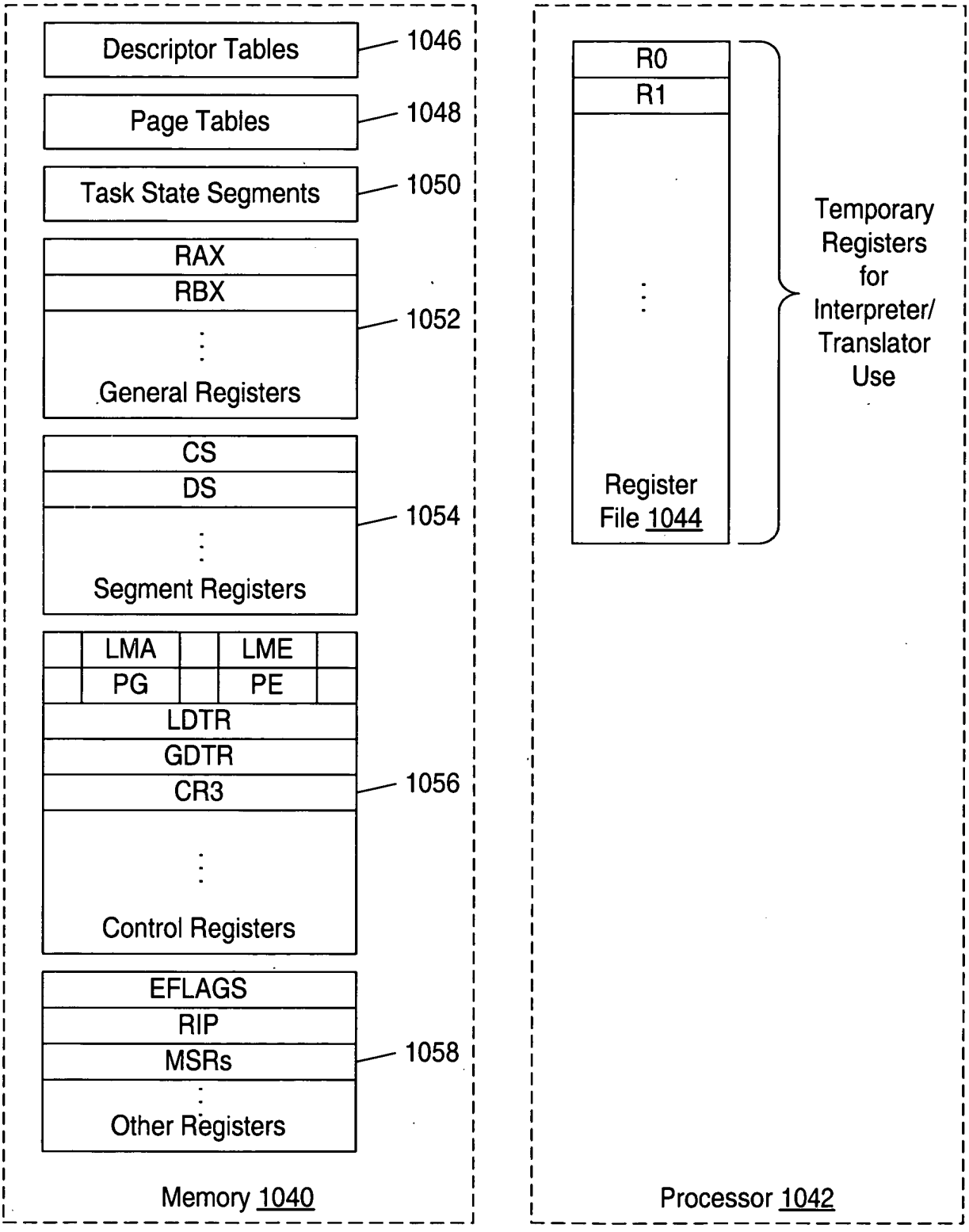
Descriptor Tables
1046
Page Tables
1048
Task State Segments
1050
RAX
RBX
General Registers
1052
CS
DS
Segment Registers
1054
LMA
LME
PG
PE
LDTR
GDTR
CR3
Control Registers
1056
EFLAGS
RIP
MSRs
Other Registers
1058
Memory 1040
R0
R1
Register File 1044
Temporary Registers for Interpreter/ Translator Use
Processor 1042

Fig. 9

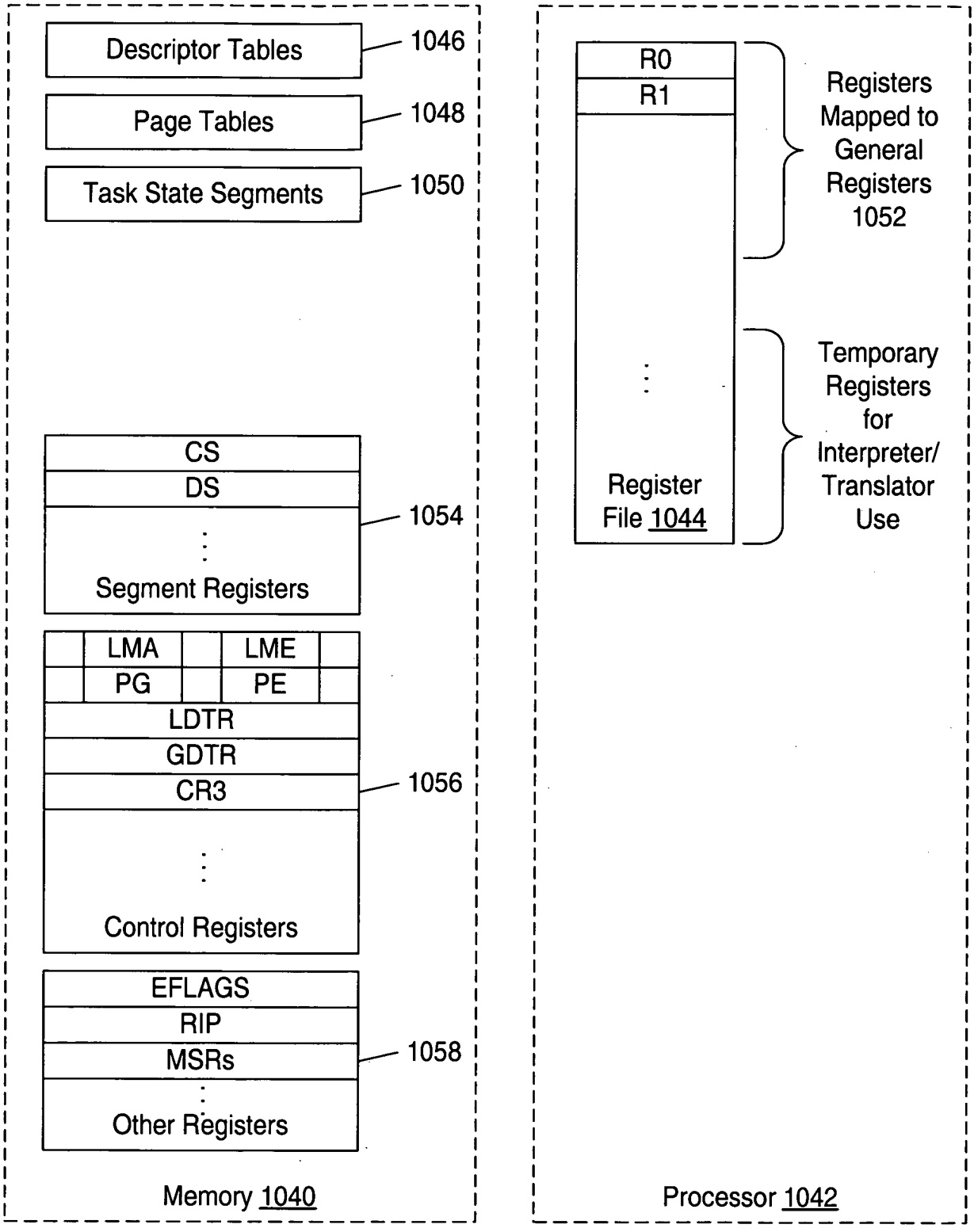
Descriptor Tables
1046
Page Tables
1048
Task State Segments
1050
CS
DS
Segment Registers
1054
LMA
LME
PG
PE
LDTR
GDTR
CR3
Control Registers
1056
EFLAGS
RIP
MSRs
Other Registers
1058
Memory 1040
R0
R1
Register File 1044
Registers Mapped to General Registers 1052
Temporary Registers for Interpreter/ Translator Use
Processor 1042

Fig. 10

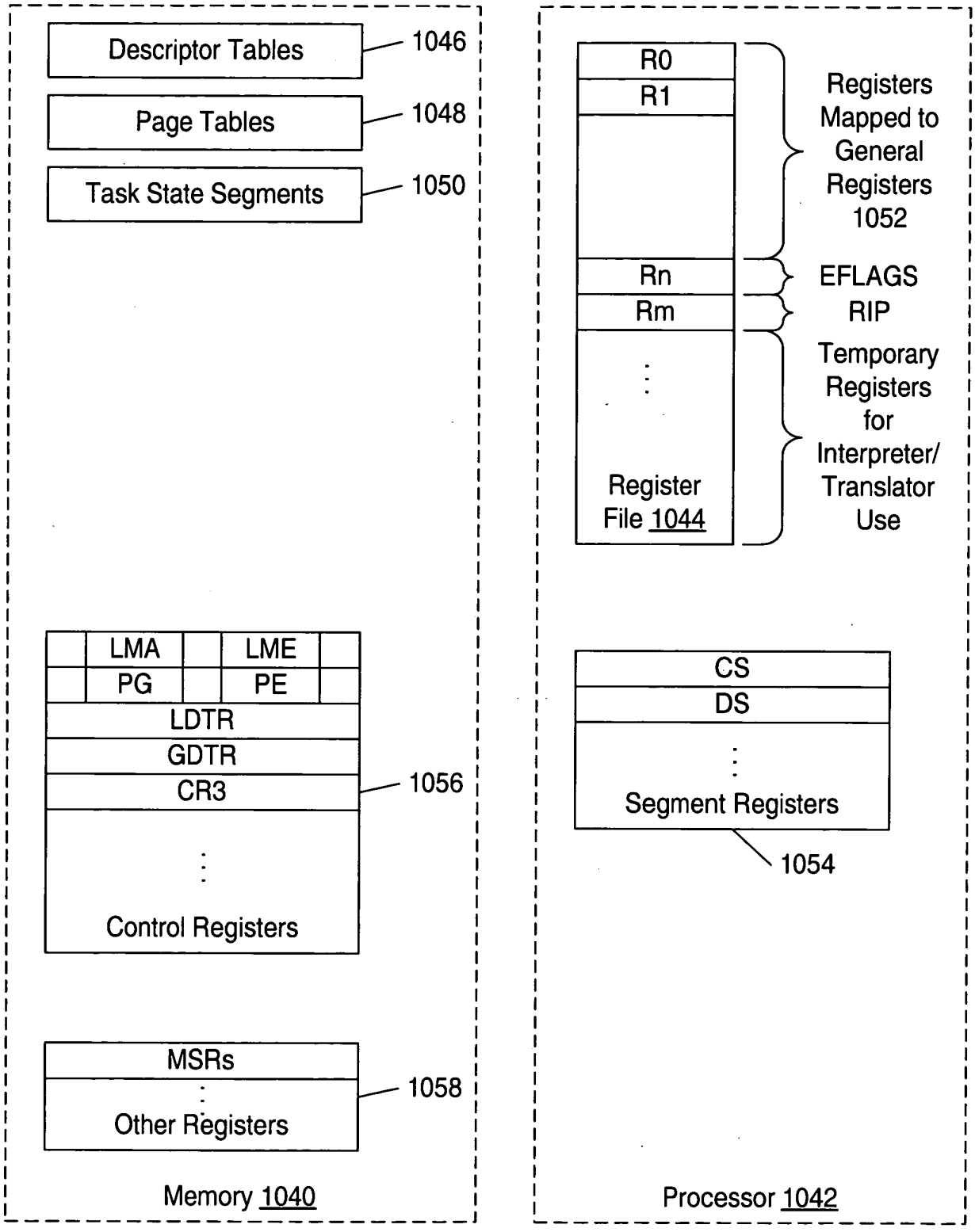
Descriptor Tables
1046
Page Tables
1048
Task State Segments
1050
LMA
LME
PG
PE
LDTR
GDTR
CR3
1056
Control Registers
MSRs
1058
Other Registers
Memory 1040
R0
R1
Registers Mapped to General Registers 1052
Rn
Rm
EFLAGS
RIP
Temporary Registers for Interpreter/ Translator Use
Register File 1044
CS
DS
Segment Registers
1054
Processor 1042

Fig. 11

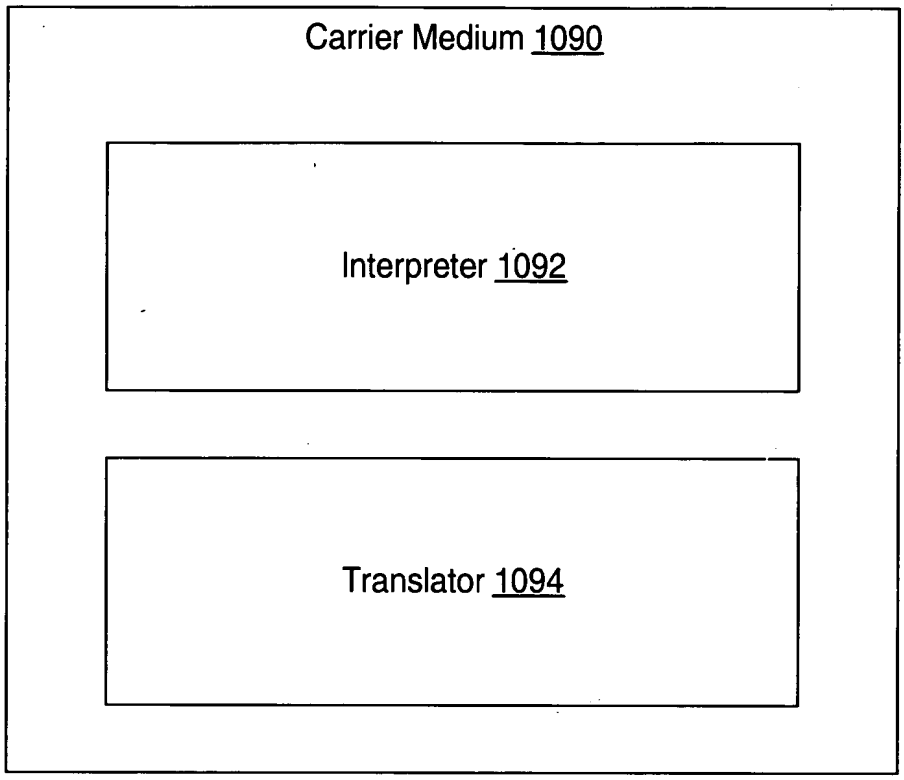

Fig. 12

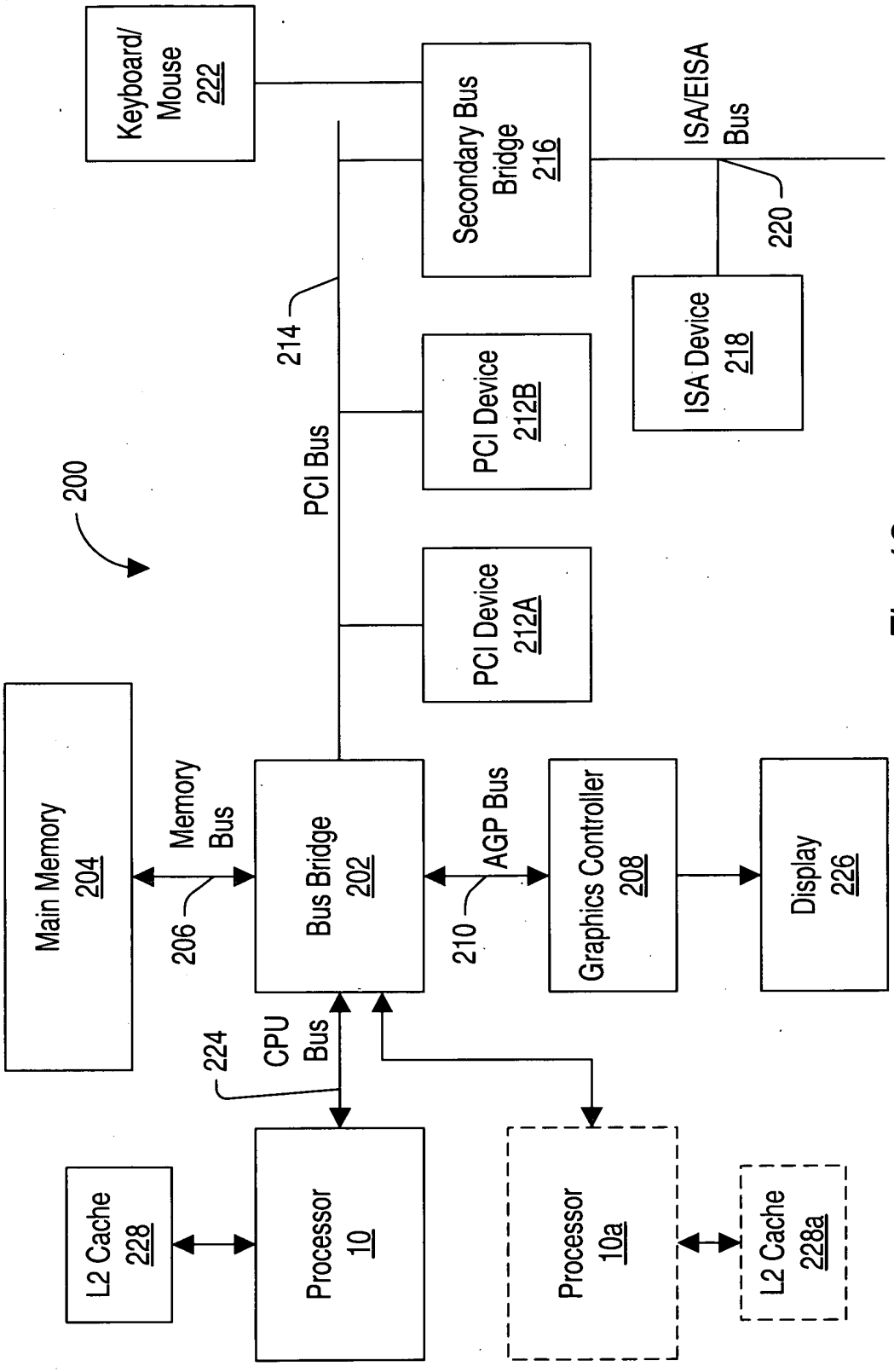
Keyboard/ Mouse 222
Secondary Bus Bridge 216
ISA/EISA Bus
220
214
PCI Bus
PCI Device 212B
ISA Device 218
200
PCI Device 212A
Main Memory 204
Memory Bus
206
Bus Bridge 202
AGP Bus
210
Graphics Controller 208
Display 226
224
CPU Bus
L2 Cache 228
Processor 10
Processor 10a
L2 Cache 228a

Fig. 13

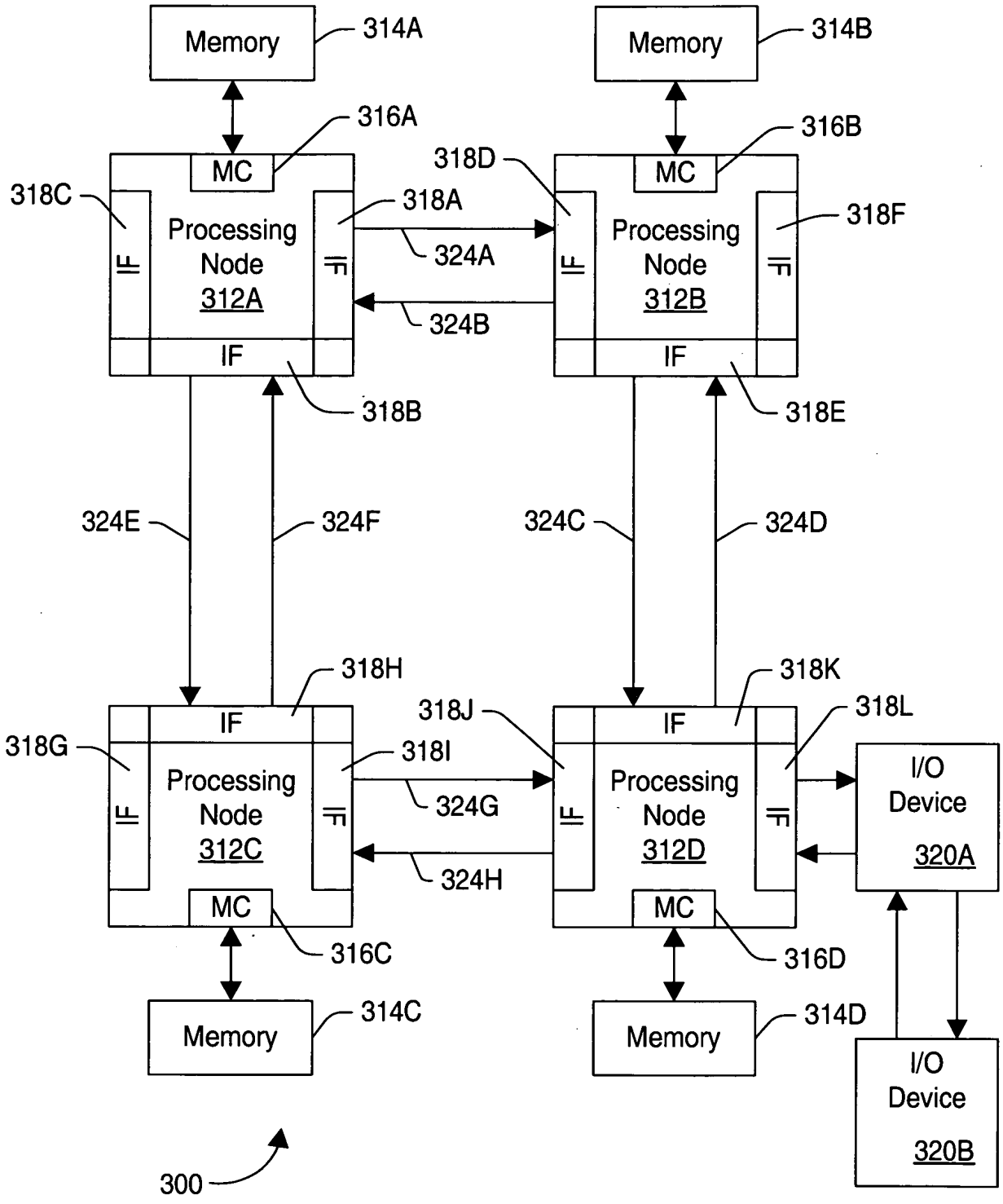
Memory
314A
Memory
314B
316A
316B
MC
MC
318C
318D
318A
318F
Processing Node 312A
Processing Node 312B
IF
IF
IF
IF
IF
IF
324A
324B
318B
318E
324E
324F
324C
324D
318H
318K
318J
318L
318G
318I
Processing Node 312C
Processing Node 312D
I/O Device 320A
324G
324H
MC
MC
316C
316D
Memory
314C
Memory
314D
I/O Device 320B
300

Fig. 14